THE INVENTION CLAIMED IS:

1. A method for failure analysis of small contacts in integrated circuits, comprising:

providing a plurality of opposing electrical contacts; and

configuring the electrical contacts to contact a sample in an offset pattern such that any one electrical contact may contact more than one conductor in the sample and any opposing electrical contact is offset-positioned to contact no more than one of the conductors contacted by the one electrical contact.

2. The method of claim 1 further comprising configuring the contacts to be offset in two perpendicular lateral directions.

3. The method of claim 2 wherein the respective offsets in the two perpendicular lateral directions are unequal and vary from contact to contact.

4. The method of claim 1 further comprising providing a parametric test structure for testing the opposing contacts.

5. The method of claim 4 further comprising using the parametric test structure to adjust the offset pattern of the contacts.

6. A method for failure analysis of small contacts in integrated circuits, comprising:

providing a plurality of opposing electrical contact arrays; and

configuring the electrical contact arrays to contact a sample in a pattern that is offset in two perpendicular lateral directions such that any one electrical contact in one of the contact arrays may contact more than one conductor in the sample and any opposing electrical contact in an opposing contact array is offset-positioned to contact no more than one of the conductors contacted by the one electrical contact.

7. The method of claim 6 wherein the respective offsets in the two perpendicular lateral directions are unequal and vary from contact to contact.

8. The method of claim 6 further comprising providing a parametric test structure for testing the opposing contacts.

9. The method of claim 8 further comprising using the parametric test structure to adjust the offset pattern of the contacts.

10. The method of claim 6 further comprising using the electrical contact arrays for at least one of:

periodically testing integrated circuits during fabrication; and

identifying at least one of the manufacturing equipment and the integrated circuits present in an operating manufacturing process.

11. A tester for failure analysis of small contacts in integrated circuits, comprising:

a plurality of opposing electrical contacts; and

means for configuring the electrical contacts to contact a sample in an offset pattern such that any one electrical contact may contact more than one conductor in the sample and any opposing electrical contact is offset-positioned to contact no more than one of the conductors contacted by the one electrical contact.

12. The tester of claim 11 wherein the contacts are offset in two perpendicular lateral directions.

13. The tester of claim 12 wherein the respective offsets in the two perpendicular lateral directions are unequal and vary from contact to contact.

14. The tester of claim 11 further comprising a parametric test structure for testing the opposing contacts.

15. The tester of claim 14 further comprising means for using the parametric test structure to adjust the offset pattern of the contacts.

16. A tester for failure analysis of small contacts in integrated circuits, comprising:

a plurality of opposing electrical contact arrays; and

means for configuring the electrical contact arrays to contact a sample in a pattern that is offset in two perpendicular lateral directions such that any one electrical contact in one of the contact arrays may contact more than one conductor in the sample and any opposing electrical contact in an opposing contact array is offset-positioned to contact no more than one of the conductors contacted by the one electrical contact.

17. The tester of claim 16 wherein the respective offsets in the two perpendicular lateral directions are unequal and vary from contact to contact.

18. The tester of claim 16 further comprising a parametric test structure for testing the opposing contacts.

19. The tester of claim 18 further comprising means for using the parametric test structure to adjust the offset pattern of the contacts.

20. The tester of claim 16 further comprising means for using the electrical contact arrays for at least one of:

periodically testing integrated circuits during fabrication; and

identifying at least one of the manufacturing equipment and the integrated circuits present in an operating manufacturing process.